AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously Presented) A method for adjusting an active filter, comprising:

providing an adjustable capacitor for determining a frequency response of said filter;

determining a measure of the frequency response and receiving a nominal frequency response;

selecting an adjustment parameter from a plurality of adjustment parameters stored in a memory arrangement based on the measure of the frequency response and the nominal frequency response; and

adjusting the adjustable capacitor on the basis of the selected adjustment parameter.

2. (Currently Amended) The method according to claim 1, wherein ~~determining~~ the measure of the frequency response of the active filter is a time constant.

3. (Previously Presented) The method according to claim 2, wherein the determined time constant is normalized to a particular value of a clock frequency used.

4. (Previously Presented) The method according to claim 1, wherein selecting from the memory arrangement uses an addressable table memory whose address has a word length comprising at least two digits, and at least one digit in the address word length is filled with a digital value derived from the determined measure of the frequency response, and at least one digit in the address word length is filled with a digital value which describes the nominal frequency response.

5. (Previously Presented) A circuit arrangement for filtering an electrical signal, comprising:

an active filter including at least one adjustable capacitor that determines frequency response;

a circuit to determine a measure of the frequency response of the active filter;

a memory arrangement which is adapted to store a plurality of adjustment parameters for adjusting the at least one adjustable capacitor; and

a control device which is adapted to select a stored adjustment parameter depending on said determined measure of the frequency response and on a nominal frequency response fed to the circuit arrangement and to adjust the at least one adjustable capacitor on the basis of the selected adjustment parameter.

6. (Original) The circuit arrangement according to claim 5, wherein the at least one adjustable capacitor includes at least one invariable base capacitor and an adjustable capacitor component.

7. (Original) The circuit arrangement according to claim 5, wherein the at least one adjustable capacitor includes a plurality of series circuits connected in parallel, which each one of the at least one adjustable capacitor comprise a single capacitor and a switch.

8. (Previously Presented) The circuit arrangement according to claim 5, wherein the memory arrangement includes a table memory for storing digital values in binary form as adjustment parameters.

9. (Previously Presented) The circuit arrangement according to claim 8, wherein the table memory includes an address word length having at least two digits, and the circuit arrangement fills at least one digit in the address word length with a digital value derived from the determined measure of the frequency response and fills at least one digit in the address word length with a digital value which describes the nominal frequency response.

10. (Original) The circuit arrangement according to claim 5, wherein the circuit arrangement is arranged to determine a time constant as a measure of the frequency response.

11. (Previously Presented) The circuit arrangement according to claim 10, wherein the circuit arrangement is arranged to normalize the time constant to a particular value of a clock frequency used when determining the time constant.

12. (Original) The circuit arrangement according to claim 5, wherein the components of the circuit arrangement are integrated into a semiconductor.

13. (Original) The circuit arrangement according to claim 5, further including at least one reference capacitor having a value in a known ratio to the value of at least one capacitor which determines frequency response, wherein the circuit for determining a measure of the frequency response of the filter is arranged to ascertain a measure of the value of the reference capacitor, and the control device is arranged to use the measure of the value of the reference capacitor instead of the measure of the frequency response of the active filter.

14. (Previously Presented) The circuit arrangement according to claim 13, wherein the reference capacitor and the capacitor which determines frequency response are made up of capacitors of the same value.

15. (Previously Presented) The method according to claim 1, wherein the nominal frequency response is selected from a plurality of given nominal frequency responses.

16. (Previously Presented) The apparatus according to claim 5, wherein the nominal frequency response is selected from a plurality of given nominal frequency responses.

17. (New) The method according to claim 1, further comprising a step of providing a fixed capacitor arranged in parallel with the adjustable capacitor.

18. (New) The method according to claim 4, wherein the digital value describing the nominal frequency response is indicative of a selected nominal frequency response taken from a set of at least two nominal frequency responses.

19. (New) The method according to claim 18, wherein the at least two nominal frequency responses have cut-off frequencies in the range from about 8 to about 12.44 MHz.

20. (New) The circuit arrangement according to claim 5, further comprising a fixed capacitor arranged in parallel with the adjustable capacitor.

21. (New) The circuit arrangement according to claim 9, wherein the digital value describing the nominal frequency response is indicative of a selected nominal frequency response taken from a set of at least two nominal frequency responses.

22. (New) The circuit arrangement according to claim 21, wherein the at least two nominal frequency responses have cut-off frequencies in the range from about 8 to about 12.44 MHz.